comprises a channel region.

[12] The semiconductor device of claim 1, wherein the gate line extends in a direction orthogonal to the direction in which the slabs extend.

[13] The semiconductor device of claim 1, wherein the gate line extends parallel to the direction in which the second active region extends.

[14] The semiconductor device of claim 1, wherein the gate line is composed of conductive polysilicon, metal, metallic nitride, or metal silicide.

[15] The semiconductor device of claim 1, wherein the gate dielectric layer contains SiO_2, SiON, Si_3N_4, $Ge_xO_yN_z$, $Ge_xSi_yO_z$, HfO_2, ZrO_2, Al_2O_3, TiO_2, or Ta_2O_5.

[16] The semiconductor device of claim 1, wherein the substrate is a silicon-on-insulator substrate comprising a buried oxide layer and a silicon layer, and the first active region and the second active region are formed on the buried oxide layer.

[17] The semiconductor device of claim 1, further comprising a first channel region and a second channel region respectively adjacent to the first surface and the second surface of each of the slabs in the first active region and facing the gate line.

[18] The semiconductor device of claim 17, further comprising a third channel region adjacent to the top surface of each of the slabs in the first active region and facing the gate line.

[19] A method of manufacturing a semiconductor, the method comprising:
forming a first active region on a substrate, the first active region being composed of a first material;
forming a second active region on the substrate, the second active region contacting at least a portion of the first active region and being composed of a second material;
forming a gate dielectric layer on the first active region; and
forming a gate on the gate dielectric layer.

[20] The method of claim 19, wherein the first active region is formed in a line-and-space pattern.

[21] The method of claim 19, wherein the first material and the second material are different from each other.

[22] The method of claim 19, wherein the forming the first active region comprises forming a plurality of slabs extending on the substrate in a first direction, each slab having a first surface, a second surface facing a direction opposite to the first side, and a top surface.

[23] The method of claim 22, wherein the top surface of each of the

that the gate line covers the fist surface, the second surface and the top surface of each of the slabs to form the gate.

[36] The method of claim 35, wherein the gate line is composed of conductive polysilicon, metal, metallic nitride, or metal silicide.

[37] The method of claim 19, further comprising preparing a silicon-on-insulator substrate as the substrate, the silicon-on-insulator substrate comprising a buried oxide layer and a monocrystalline silicon layer formed on the buried oxide layer, and the first active region is formed by patterning the monocrystalline silicon layer.